PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE LAI et al.

Application for Patent

Filed March 07, 2001

Serial No. 09/801,350

FOR:
ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT COUPLED ON I/O PAD

APPEAL BRIEF
(Amended)

CERTIFICATE OF MAILING

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Signature: _____
JIAWEI HUANG, Reg. No. 43,330

JC PATENTS
Representatives for Applicants

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I. REAL PARTY IN INTEREST

The real parties in interest are Chun-Hsiang Lai, Meng-Huang Liu and Tao-Tseng Lu, the inventors named in the subject application, and Macronix International Co., Ltd., the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

A Pre-Appeal Brief Request for Review was filed on July 27, 2005 in connection with the present application (09/801,350). A copy of Notice of Panel Decision from Pre-appeal Brief Review is enclosed herewith.

III. STATUS OF THE CLAIMS

A total of 6 claims were presented during prosecution of this application. Applicant appeals rejected claims 1-4, 13 and 15.

IV. STATUS OF THE AMENDMENTS

Applicant did not file any Amendments after Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The conventional I/O pad ESD protection circuit comprises two transistors. When the voltage from the I/O pad is exported to an internal circuit, an ESD protection circuit usually is involved in design to prevent an over voltage from occurring and affecting the operation of the internal circuit, the two transistors can discharge electrostatic charges away when the over positive voltage or over negative voltage occur on the I/O pad. In addition, a low-voltage triggering silicon-controlled rectifier (LVTSCR) is also included,

which is used to further enhance the discharge rate. However, when a current (I) supplied to the I/O pad exceeds the minimum working current (I_H) i.e. $I>I_H$, a latch-up would occur, causing the function of the ESD protection circuit to be temporarily or permanently fail.

In order to resolve the above defects of the conventional ESD protection circuit, the present Inventors provides an anti-latch-up circuit, and propose to electrically connect the anti-latch-up circuit to the SCR circuit which is electrically connected to the I/O pad. The anti-latch-up circuit is designed to prevent activation of the SCR circuit during the normal IC operation. The SCR circuit comprises a first connection terminal, a second connectional terminal and a third connectional terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage; and the anti-latch-up circuit comprises a fourth connection terminal, a fifth connection terminal and a sixth connection terminal respectively connected to the voltage source, the ground voltage and the third connection terminal of the SCR circuit (as recited by claim 1). According to the claimed invention, the advantage of connecting the (fourth connection terminal of) anti-latch-up circuit to the voltage source and the first connection terminal of the SCR circuit to the I/O pad is that only one anti-latch-up circuit is required for several I/O pads, and therefore, the space occupation on the integrated circuit can be effectively reduced. In other words, if the fourth connection terminal is connected to the I/O pad instead of the voltage source, then one anti-latch-up circuit is required for each of the I/O pads and thus the space occupation on the integrated circuit will be increased.

Furthermore, the present Inventors propose a RC DELAY TIME of the anti-latch up circuit to be smaller than a voltage rising time of the IC power but greater than the voltage rising ESD pulse (as recited in claim 15). Accordingly, when there is an accidental over-voltage or voltage surge during the normal IC operation, because the RC Delay Time of the anti-latch up circuit is designed to be smaller than a voltage rising time of

the IC power, therefore the rising voltage of the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power so that a voltage level of the node A has the same voltage (Vdd). Thus, a large amount of carriers, due to accidental over voltage, may be accordingly absorbed and the latch-up phenomenon is avoided. On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, therefore the rising voltage of the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit. Therefore the SCR circuit may be triggered at a lower holding voltage. Thus, the anti-latch-up circuit of the present invention may be effectively utilized for effectively preventing the latching up phenomenon during the normal IC operation.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 3, 4 and 13 were rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US-5,982,601, hereinafter Lin).

B. Claims 1, 3-4, 13 and 15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley et al. (US-5,781,388, hereinafter Quigley) in view of Lin.

C. Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Quigley and Lin as applied to claim 1, and further in view of Ker et al. (US-5,754,380, hereinafter Ker).

D. Claim 15 was rejected under 35 USC 103(a) as being unpatentable over Lin.

E. Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Lin in view of Ker.

VII. ARGUMENT

A. The related law

A prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

Finally, if an independent claim is nonobvious under 35 U.S.C. 103 (or unanticipated under 35 U.S.C. 102), then any claim depending therefrom is nonobvious (or unanticipated). *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. *Claims 1, 3, 4 and 13 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US-5,982,601, hereinafter Lin).*

1. The rejection

The Examiner rejected claims 1, 3, 4 and 13 as being anticipated by Lin. The Examiner stated that Lin teaches in Figure 9 and related text an ESD protection circuit for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit (FIG. 6), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal

and the second connection terminal are respectively connected to the I/O pad (Anode) and a ground voltage (Cathode), so as to discharge the electrostatic charges; and an anti-latch-up circuit 51, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal A, respectively coupled to a voltage source (the pad line), the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit A is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation.

2. The prior art

Lin, at FIG. 6A and 9, discloses an ESD protection circuit including a SCR circuit and a transient oscillator circuit 61 for generating fast clocks during an ESD transient. Lin substantially discloses that the transient oscillator circuit 61 is respectively connected to the VDD bus or the I/O pad, the SCR circuit and the ground (VSS bus), and the SCR is respectively connected to the VDD bus or the I/O pad and the ground (VSS bus).

Furthermore, Lin, at col. 3, lines 48-53, substantially discloses that the transient oscillator circuit 61 is employed for generating fast clocks with increasing oscillation amplitude during the initial phase of an ESD transient. Also, the voltage transition of the fast clocks has a ramp rate faster than the ESD transient voltage's ramp rate.

3. The prior art distinguished

It is well established that rejection under 35 U.S.C. 102 requires that each and every elements of the rejected claim must be exactly disclosed by a single prior art reference.

Lin cannot anticipate the proposed independent claim 1 because Lin fails to teach, disclose or show each and every elements of the proposed independent claim 1.

More specifically, the Applicants respectfully submit that Lin fails to teach or disclose that the first connection terminal and the second connection terminal of the SCR circuit are respectively connected to the I/O pad and a ground voltage, and the fourth connection terminal, the fifth connection terminal, and the sixth connection terminal of the anti-latch-up circuit are respectively coupled to the voltage source, the ground voltage, and the third connection terminal of the SCR circuit as recited by the proposed independent claim 1. Instead, Lin substantially discloses that the Three connection terminals of the transient oscillator circuit 61 are respectively connected to the VDD bus or the I/O pad, the SCR circuit and the ground (VSS bus), and the Three connection terminals of the SCR circuit are respectively connected to the VDD bus or the I/O pad and the ground (VSS bus) and the transient oscillator circuit 61 (please see FIG. 6A and 9). In other words, as clearly shown in FIG. 6A and 9, Lin substantially shows that the connection terminals of both transient oscillator circuit 61 and the SCR circuit are connected to the VDD bus or the I/O pad. Therefore, it is clearly evident that Lin substantially fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient circuit is connected to the voltage source, instead Lin substantially teaches or discloses that the connection terminals of BOTH transient oscillator circuit 61 and SCR circuit are connected to the same VDD bus or the same I/O PAD.

The Examiner has misinterpreted that the first connection terminal of the SCR circuit of Lin is connected to the I/O pad and the transient oscillator circuit 61 of Lin is connected to the voltage source or the pad line. In other words, the Examiner has misinterpreted that the pad line as TWO SEPARATE ELEMENTS, NAMELY, THE I/O PAD AS WELL AS THE VOLTAGE SOURCE. However, the Figure 6A and 9 of Lin, and the related text, very clearly shows that the (first) connection terminal of the SCR circuit and the (fourth) connection terminal of the transient oscillator circuit 61 are respectively connected to the SAME VDD bus or the SAME I/O Pad. Therefore, the Examiner has misinterpreted that the first connection terminal of the SCR circuit of Lin is connected to the I/O pad and the fourth connection terminal of the transient oscillator circuit 61 of Lin is connected to the voltage source or the pad line, which is different from I/O pad.

In the claimed invention, as clearly recited in claim 1, and also as clearly shown in Figure 4, the first connection terminal (112) of the SCR circuit (104) is connected to "a I/O pad" (100); and the fourth connection terminal (126) of the anti-latch-up

circuit (110) is connected to "a voltage source" (Vcc). The language "the first connection terminal (112, of the SCR circuit) is connected to a I/O pad" and "the fourth connection terminal (126) of the anti-latch-up circuit) is coupled to a voltage source (Vcc)" clearly indicate that the I/O PAD and the VOLTAGE SOURCE are TWO SEPARATE ELEMENTS, and that the first connection terminal of the SCR circuit and the fourth connection terminal of the anti-latch-up circuit are respectively connected to DIFFERENT ELEMENTS, namely, the I/O PAD and the VOLTAGE SOURCE, which is also fully supported by Figure 4.

The advantage of connecting the (fourth connection terminal of the) anti-latch-up circuit to the voltage source and connecting the (first connection terminal of the) SCR circuit to the I/O pad is that only one anti-latch-up circuit is required for several I/O pads, and therefore, the space occupation on the integrated circuit can be effectively reduced.

Because Lin substantially teaches that the connection terminals of BOTH transient oscillator circuit 61 and SCR circuit are connected to the SAME VDD bus or the SAME I/O PAD, and therefore one transient circuit is required for each of the VDD bus or the I/O pad. In other words, Lin because fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient oscillator circuit 61 is connected to the voltage source.

Thus, the structure of the ESD protection device of Lin is substantially different compared to the structure of the ESD protection device of the present invention.

Accordingly, Lin cannot possibly anticipate the proposed independent claim 1, and therefore the proposed independent claim 1 patentably defines over Lin, and should be allowed.

Also, the remaining claims 3, 4 and 13 depend directly or indirectly from the proposed independent claim 1, and therefore patentably define over Lin for at least the reasons recited above.

C. *Claims 1, 3-4, 13 and 15 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley et al. (US-5,781,388, hereinafter Quigley) in view of Lin.*

1. The rejection

The Examiner rejected claims 1, 3-4, 13 and 15 as being unpatentable over Quigley in view of Lin. The Examiner stated that regarding claims 1 and 13, Quigley teaches in Figure 1 an ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit 22, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage (Vss), so as to discharge the electrostatic charges; and an anti-latch-up circuit RC 17, 18, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal 21, respectively coupled to a voltage source (the pad line), the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit 21 is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation. Although Quigley does not state a voltage source, this feature is inherent in Quigley's device as the line connected to the pad is the voltage source to the device. Further, capacitor C also provides a voltage source to the device. Note that the device would not function without a voltage source.

Furthermore, Quigley does not explicitly state that the voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit. Lin teaches in Figures 6, 9 and 10 and related text a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during the normal operation in Quigley's device, in order to improve the protection capabilities of the device.

Furthermore, regarding claim 15, the Examiner stated that it would have been obvious to a person skilled in the art at the time the invention was made to use a

RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse in Quigley's device in order to improve the protection capability of the device.

2. The prior art

The disclosure of Lin is discussed above.

Quigley, at Figure 1, substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the SAME I/O PAD.

Quigley, at col. 4, lines 41-62, substantially teaches that because gate oxide breakdown occurs when a 10 volt DC voltage is applied across the gate oxide or a 20 volt transient voltage, and therefore ESD protection circuit 11 must enable SCR circuit 22 before the pad reaches 20 volts because an ESD event is a transient phenomenon corresponding to the higher voltage for gate oxide breakdown. More particularly, Quigley, at col. 4, lines 50-62, substantially teaches that the transistor 16 is enabled for turning on transistor 12 when a voltage at node 21 exceeds the threshold voltage of the transistor 16 and thereby generates a voltage at the node 21 to trigger the SCR circuit 22. Thus, Quigley substantially proposes setting a threshold voltage of, for example, 12 volts, as trigger voltage at the pad, and when the voltage at the pad exceeds 12 volts, the SCR circuit 22 is triggered. Quigley utilizes a voltage divider circuit, including a capacitor 17 and a resistor 18, designed for generating a control voltage to SCR circuit 22 due to a transient voltage applied to the pad when the voltage at the pad exceeds threshold voltage 12 volts.

Furthermore, Quigley, at col. 7, lines 1-4, substantially teaches that to sufficiently prolong the delay time of the SCR circuit 22 to prevent normal signals of the integrated circuit from triggering the SCR circuit 22.

3. The prior art distinguished

Quigley, like Lin, at Figure 1, substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the I/O PAD. In other words, Quigley fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient circuit is connected to the voltage source, instead, Quigley substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the SAME I/O PAD. Therefore one voltage divider (17 and 18) is required for each of the I/O pads.

The Examiner has misinterpreted that the first connection terminal of the SCR circuit of Quigley is connected to the I/O pad and the voltage divider (17 and 18) of Quigley is connected to the voltage source or the pad line. In other words, the Examiner has misinterpreted that the pad line as TWO SEPARATE ELEMENTS, NAMELY, THE I/O PAD AS WELL AS THE VOLTAGE SOURCE. However, the Figure 1 of Quigley, and the related text, very clearly shows that the (first) connection terminal of the SCR circuit and the (fourth) connection terminal of the voltage divider are respectively connected to the SAME I/O Pad. Therefore, the Examiner has misinterpreted that the first connection terminal of the SCR circuit of Quigley is connected to the I/O pad and the fourth connection terminal of the voltage divider of Quigley is connected to the voltage source or the pad line, which is different from I/O pad.

In the claimed invention, as clearly recited in claim 1, and also as clearly shown in Figure 4, the first connection terminal (112) of the SCR circuit (104) is connected to "a I/O pad" (100); and the fourth connection terminal (126) of the anti-latch-up circuit (110) is connected to "a voltage source" (Vcc). The language "the first connection terminal (112, of the SCR circuit) is connected to a I/O pad" and "fourth connection terminal (126, of the anti-latch-up circuit) is coupled to a voltage source (Vcc)" clearly indicate that the I/O PAD and the VOLTAGE SOURCE are TWO SEPARATE ELEMENTS, and that the first connection terminal of the SCR circuit and the fourth connection terminal of the anti-latch-up circuit are respectively connected to DIFFERENT ELEMENTS, namely, the I/O PAD and the VOLTAGE SOURCE, which is also fully supported by Figure 4.

The advantage of connecting the (fourth connection terminal of the) anti-latch-up circuit to the voltage source and connecting the (first connection terminal of the) SCR circuit to the I/O pad is that only one anti-latch-up circuit is required for several I/O pads, and therefore, the space occupation on the integrated circuit can be effectively reduced.

Because Quigley substantially teaches that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit (22) are connected to the SAME the SAME I/O PAD, and therefore one voltage divider (17 and 18) is required for each of the I/O pads. In other words, Lin because fails to teach, disclose or suggest that the first connection terminal of the SCR circuit (22) is connected to the I/O pad and the fourth connection terminal of the voltage divider (17 and 18) is connected to the voltage source.

Thus, the structure of the ESD protection device of Quigley is substantially different compared to the structure of the ESD protection device of the present invention.

Accordingly, the combination of Quigley and Lin, in a manner suggested by the Examiner, cannot possibly render every features of the proposed independent claim 1 obvious in this regard, and therefore the proposed independent claim 1 patentably defines over Quigley and Lin and should be allowed.

Also, the remaining claims 3, 4 and 13 depend directly or indirectly from the proposed independent claim 1, and therefore patentably define over Quigley and Lin for at least the reasons cited above.

Furthermore, REGARDING CLAIM 15, the Examiner stated that it would have been obvious to a person skilled in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse in Quigley's device in order to improve the protection capability of the device.

Applicants would like to particularly point out that the feature recited in claim 15, in fact, further distinguishes the claimed invention from the prior art references Quigley and Lin. Claim 15 recites the limitation "a RC DELAY TIME of the anti-latch up circuit smaller than a voltage rising time of the IC power but greater than the voltage rising

ESD pulse". According to the present invention, when there is an accidental over-voltage or voltage surge during the normal IC operation, because the RC Delay Time of the anti-latch up circuit is designed to be smaller than a voltage rising time of the IC power, therefore the rising voltage of the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power so that a voltage level of the node A has the same voltage (Vdd). Thus, a large amount of carriers, due to accidental over voltage, may be accordingly absorbed and the latch-up phenomenon is avoided. On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, therefore the rising voltage of the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit. Therefore the SCR circuit may be triggered at a lower holding voltage.

Instead, Quigley, at col. 4, lines 41-62, substantially teaches that because gate oxide breakdown occurs when a 10 volt DC voltage is applied across the gate oxide or a 20 volt transient voltage, and therefore ESD protection circuit 11 must enable SCR circuit 22 before the pad reaches 20 volts because an ESD event is a transient phenomenon corresponding to the higher voltage for gate oxide breakdown. More particularly, Quigley, at col. 4, lines 50-62, substantially teaches that the transistor 16 is enabled for turning on transistor 12 when a voltage at node 21 exceeds the threshold voltage of the transistor 16 and thereby generates a voltage at the node 21 to trigger the SCR circuit 22. Thus, Quigley substantially proposes setting a threshold voltage of, for example, 12 volts, as trigger voltage at the pad, and when the voltage at the pad exceeds 12 volts, the SCR circuit 22 is triggered. Quigley utilizes a voltage divider circuit, including a capacitor 17 and a resistor 18, designed for generating a control voltage to SCR circuit 22 due to a transient voltage applied to the pad when the voltage at the pad exceeds threshold voltage 12 volts.

Furthermore, Quigley, at col. 7, lines 1-4, substantially teaches that to sufficiently prolong the delay time of the SCR circuit 22 to prevent normal signals of the integrated circuit from triggering the SCR circuit 22.

Therefore, it is clear that the mechanism of preventing triggering and triggering of the SCR circuit of the claimed invention is substantially different from that of Quigley, in that the claimed invention does not set any threshold voltage for triggering the SCR circuit or prolong the delay time of the SCR circuit to prevent normal signals of the IC from triggering the SCR circuit as expressly taught by Quigley, instead the claimed invention proposes designing the RC Delay Time of the anti-latch-up circuit to be smaller than the voltage rising of the IC power but greater than the rising voltage time of the ESD pulse so that the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power to prevent triggering the SCR circuit , and during the ESD event, the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit.

Accordingly, Applicants respectfully submit that Quigley SUBSTANTIALLY TEACHES AWAY from the claimed invention, and therefore Quigley cannot possibly suggest one skilled in the art to modify Quigley's ESD device in a manner suggested by the Examiner because any such modification of Quigley's device would frustrate its intended purpose. As such, Quigley is complete and functional in itself, so there would be no reason to modify ESD circuit of Quigley, and certainly not to modify the voltage divider of Quigley in the manner suggested only by the Examiner. Applicants respectfully submit that it is impermissible, however simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from

references to fill the gaps, and any such reconstruction to depreciate the claimed invention would be construed as hindsight reconstruction.

Accordingly, Quigley, in a manner suggested by the Examiner, cannot possibly meet claim 15, and therefore claim 15 patentably defines over Quigley.

D. *Claim 2 was improperly rejected under 35 USC 103(a) as being unpatentable over Quigley and Lin as applied to claim 1 above, and further in view of Ker et al. (US-5,754,380, hereinafter Ker).*

1. The rejection

The Examiner rejected claim 2 as being unpatentable over Quigley and Lin, and in further view of Ker. The Examiner stated that Quigley and Lin substantially teaches the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source. Ker teaches in Figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source in the device of Quigley and Lin in order to provide a better protection for the device against ESD event.

2. The prior art

The disclosures of Quigley and Lin are discussed above.

Ker substantially teaches an ESD protection circuit for use in a CMOS output buffer circuit has been disclosed. The ESD protection circuit provides a high ESD failure threshold in a small layout area to protect the output buffer against ESD failure. The

output buffer includes a pull-up PMOS device and pull-down NMOS device whose common drain is connected to an output pad. The source of the PMOS device is connected to VDD and the source of NMOS device is connected to VSS. The ESD protection circuit is formed by a PTLSCR device and an NTLSCR device. The PTLSCR (NTLSCR) is formed by inserting a short-channel thin-oxide PMOS (NMOS) device into a lateral SCR structure. These MOS devices reduce the turn-on voltage of the lateral SCR to the snapback breakdown voltage of the MOS rather than the original switching voltage of the SCR. The ESD protection circuit also includes two parasitic diodes (60 and 70) between output pad and VDD and Dn between output pad and VSS. The four modes of ESD, PS, NS, PD and ND, are one-by-one protected by NTLSCR, Dn, Dp and PTLSCR, respectively.

3. The prior art distinguished

Applicants respectfully submit that the first diode 70 and the second diode 60 of Ker still cannot cure the specific deficiencies of Lin for at least the same reasons discussed above. Therefore, Applicants respectfully submit that claim 2 also patently defines over Lin and Ker, and claim 2 should be allowed.

E. *Claim 15 was improperly rejected under 35 USC 103(a) as being unpatentable over Lin.*

1. The rejection

The Examiner rejected claim 15 as being unpatentable over Lin. The Examiner stated that Lin substantially teaches the entire claimed structure, as applied to claim 1 above, including a RC delay time of the anti-latch-up circuit being greater than a voltage rising time of the ESD pulse.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit being

smaller than a voltage rising time of an IC power in Lin's device in order to operate the device in its intended use.

2. The prior art

The disclosure of Lin is discussed above.

More particularly, Lin, at col. 3, lines 48-53, substantially discloses that the transient oscillator circuit 61 is employed for generating fast clocks with increasing oscillation amplitude during the initial phase of an ESD transient, and also, the voltage transition of the fast clocks has a ramp rate faster than the ESD transient voltage's ramp rate.

3. The prior art distinguished

Applicants respectfully submit that because Lin, at col. 3, lines 48-53, substantially discloses that the transient oscillator circuit 61 is employed for generating fast clocks with increasing oscillation amplitude during the initial phase of an ESD transient, and also, the voltage transition of the fast clocks has a ramp rate faster than the ESD transient voltage's ramp rate.

Therefore, it clear that Lin substantially fails to teach, suggest or hint that the anti-latch-up circuit has a RC delay time that is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as required by the dependent claim 15, instead, Lin substantially teaches the voltage transition provided by the voltage transition circuit (51) has a ramp rate faster than the ESD voltage's ramp rate. In other words, because Lin substantially teaches the voltage transition has RC delay time SMALLER THAN the ESD VOLTAGE'S RAMP RATE, therefore, it is clearly evident that Lin substantially teaches away from the claimed invention in this regard.

Accordingly, Lin cannot possibly meet the proposed claim 15 in this regard, and therefore the proposed claim 15 should be allowed.

F. Claim 2 was improperly rejected under 35 USC 103(a) as being unpatentable over Lin in view of Ker.

1. The rejection

The Examiner rejected claim 2 as being unpatentable over Lin in further view of Ker. The Examiner stated that Lin substantially teaches the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source. Ker teaches in Figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source in the device of Lin in order to provide a better protection for the device against ESD event.

2. The prior art

The disclosures of Lin and Ker are discussed above.

3. The prior art distinguished

Applicants respectfully submit that the first diode 70 and the second diode 60 of Ker still cannot cure the specific deficiencies of Lin for at least the same reasons discussed above. Therefore, Applicants respectfully submit that claim 2 also patently defines over Lin and Ker, and claim 2 should be allowed.

G. CONCLUSION

As noted, none of the cited art, either alone or in combination, can be said to anticipate or render obvious the appealed claims. The references disclosing ESD protection circuit (Quigley, Lin, and Ker) fail to disclose, show, or suggest the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient circuit is connected to the voltage source (as recited in claim 1). Also, these references fail to disclose, show, or suggest ", and a RC delay time of the anti-latch up circuit smaller than a voltage rising time of the IC power but greater than the voltage rising ESD pulse (as recited in claim 15)". The addition of Ker showing the first diode 70 and the second diode 60 is prior art, but does not cure the deficiencies of Lin and Quigley with respect to the connections of the transient circuit and the voltage divider respectively with respect to the I/O pad as discussed above.

Accordingly, Applicant believes that the rejections under 35 U.S.C. 102 and 103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,
J.C. PATENTS

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APPENDIX A - CLAIMS ON APPEAL

Claim 1. (Previously Presented) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation.

Claim 2. (Original) The ESD protection circuit of claim 1, further comprising:

a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and

a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Claim 3. (Previously Presented) The ESD protection circuit of claim 1, wherein the SCR circuit comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends the anti-latch-up signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and

a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source;

wherein a diode is coupled to the second P+ doped region and the I/O pad at one end and coupled to the other end.

Claim 4. (Original) The ESD protection circuit of claim 3, wherein the anti-latch-up circuit comprises:

a capacitor, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

Claims 5-12 (Canceled).

Claim 13. (Previously Presented) The ESD protection circuit of claim 1, wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Claim 14 (Canceled).

Claim 15. (Previously Presented) The ESD protection circuit of claim 1, wherein a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse.